

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs



Figure 13 Single-Supply DAC Transfer Function

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX530A0EAG	-40°C to +85°C	24 Narrow Plastic DIP	$\pm \frac{1}{2}$
MAX530B0EAG	-40°C to +85°C	24 Narrow Plastic DIP	$\pm \frac{1}{2}$
MAX530A0EAG	-40°C to +85°C	24 Wide SO	$\pm \frac{1}{2}$
MAX530B0EAG	-40°C to +85°C	24 Wide SO	$\pm \frac{1}{2}$
MAX530A0EAG	-40°C to +85°C	24 SSOP	$\pm \frac{1}{2}$
MAX530B0EAG	-40°C to +85°C	24 SSOP	$\pm \frac{1}{2}$
MAX530A0MRG	-55°C to +125°C	24 Narrow QFP ¹	± 1
MAX530B0MRG	-55°C to +125°C	24 Narrow QFP ¹	± 1

... Contact factory for availability and processing to MIL-STD-883. ±2

General Description

General Description

The MAX538's buffer is fixed at a gain of 1 and the MAX539's buffer at a gain of 2. The MAX531's internal op amp may be configured for a gain of 1 or 2, as well as for unipolar or bipolar output voltages. The MAX531 can also be used as a four-quadrant multiplier without external resistors or op amps.

For parallel data inputs, see the MAX530 data sheet.

Applications

Battery-Powered Test Instruments

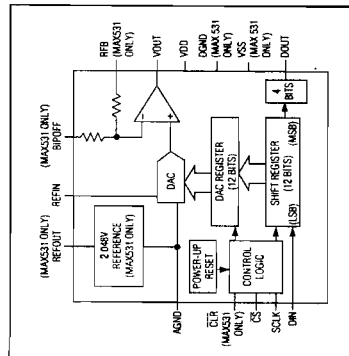
Digital Offset and Gain Adjustment

Battery-Operated/Remote Industrial Controls

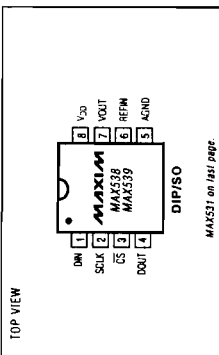
Machine and Motion Control Devices

Cellular Telenhones

Functional Diagram



Pin Configurations



3-23a

MAXIM

MAXIM

MAXIM _____ **MAX**
Call toll free 1-800-998-8800 for free samples or literature.

Maxim Integrated Products 9-39

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

	Continuous Power Dissipation ($T_A = 70^\circ\text{C}$)	0°C to $+70^\circ\text{C}$
V _{DD} to DGND and V _{SS} to AGND	8-Pin Static DIP (derate 9.0mW/°C above $+70^\circ\text{C}$)	721mW
V _{SS} to DGND and V _{SS} to AGND	8-Pin Static DIP (derate 5.0mW/°C above $+70^\circ\text{C}$)	471mW
V _{DD} to DGND and V _{DD} to AGND	8-Pin CERDIP (derate 9.0mW/°C above $+70^\circ\text{C}$)	721mW
V _{DD} to DGND and V _{DD} to AGND	8-Pin Plastic DIP (derate 9.0mW/°C above $+70^\circ\text{C}$)	800mW
V _{DD} to DGND and V _{DD} to AGND	14-Pin SO (derate 8.33mW/°C above $+70^\circ\text{C}$)	600mW
V _{DD} to DGND and V _{DD} to AGND	14-Pin SO (derate 8.33mW/°C above $+70^\circ\text{C}$)	600mW
V _{DD} to DGND and V _{DD} to AGND	14-Pin CERDIP (derate 9.0mW/°C above $+70^\circ\text{C}$)	721mW
V _{DD} to DGND and V _{DD} to AGND	Operating Temperature Ranges:	
V _{DD} to DGND and V _{DD} to AGND	MAX332 - C	-40°C to $+70^\circ\text{C}$
V _{DD} to DGND and V _{DD} to AGND	MAX332 - E	-40°C to $+70^\circ\text{C}$

Note 1: The output may be shorted to V_{DD} , V_{SS} , or AGND if the package power dissipation limit is not exceeded. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to maximum junction temperature above 150°C may affect device reliability.

MAX531). $R_L = 10k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution						
Relative Accuracy (Note 2)	N	MAX53_AOE MAX53_AM	12		+0.5	Bits
		MAX53_BOE		±1		LSB
		MAX53_BMI		±1		
		Guaranteed monotonic		±2		
Differential Nonlinearity	DNL				±1	LSB
Injurious Offset Error (Note 3)	VOS				±1	LSB
Injurious Offset Tempco	TCVos		0		4	LSB
Gain Error (Note 2)	GE	MAX53_OIE	3			ppm/V
		MAX53_IM			±1	LSB
Power-Supply Rejection Ratio, Injurious Offset Error and Gain error	PSRR			1	±2	ppm/V
ALTAGE OUTPUT (Vout)						
Output Load Regulation	V _{SC}	MAX531(G = 1), MAX538	0		V _{DD} -2	V
		MAX531(G = 2), MAX539	0		V _{DD} -0.4	V
		VOUT = 2V, I _L = 2kΩ			-1	LSB
REFERENCE INPUT (REFIN)				12		mA
Voltage Range						
Input Resistance			0		V _{DD} -2	V
Input Capacitance			40		I _Q	pF
Freethrough			10		50	pF
			-80			dB

$V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $AGND = DGND = 0V$, $REFIN = 2.048V$ (external), $REFB = BIPOFF = V_{OUT}$ (MAX531), $CREFOUT = 33\mu F$ (MAX531), $R_L = 10k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE OUTPUT (REFOUT – MAX531 only)						
Reference Output Voltage		V _{DO} = 5.0V (Note 6)		2.024 2.017 2.013	2.048 2.079 2.083	V
		MAX531BC				
		MAX531BE				
Temperature Coefficient	T _{REFOUT}	MAX531AC/AE/AM/BM		15	50	ppm/°C
		MAX531BIC/BE		15	2	°C
Resistance	REFOUT	(Note 5)		0.5	2	Ω
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V _{DO} ≤ 5.5V			300	μV/V
Noise Voltage	en	0.1Hz to 10kHz			400	nV/√p
Minimum Required External Capacitor	C _{MIN}		3.3			μF
DIGITAL INPUTS (DIN, SCLK, CS, CLR)						
Input High	V _{IH}		2.4			V
Input Low	V _{IL}			0.8		V
Input Current	I _{IN}	V _{IN} = 0V or V _{DD}		±1		μA
Input Capacitance	C _{IN}			8		pF
DIGITAL OUTPUT (DOUT)						
Output High	V _{OH}	I _{SOURCE} = 2mA	V _{DD} - 1			V
Output Low	V _{OL}	I _{SINK} = 2mA		0.4		V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR	T _A = +25°C	0.15	0.25		V/μs
Voltage-Output Settling Time	t _{OSHO}	T _A to 1/2LSB, V _{OUT} = 2V		25		μs
Digital Feedthrough	CSH	CS = V _{DD} , DIN = 100kHz		5		nV/s
Signal-to-Noise plus Distortion	SINAD	REFIN = 1kHz, 2V _{p-p} (G = 1 or 2), Code = FFFF _{hex}		68		dB
POWER SUPPLY						
Positive Supply Voltage	V _{DD}		4.5	5.5		V
Power-Supply Current	I _{DD}	All inputs = 0V or V _{DD} , output = no load		260 140	400 300	μA
SWITCHING CHARACTERISTICS						
CS Setup Time	t _{CSSS}		20			ns
SCLK Fall to CS Fall Hold Time	t _{CSHF}		15			ns
ICSH			0			ns
SCLK Fall to CS Rise Hold Time	t _{CSH1}		35			ns
ICSH			35			ns
SCLK Low Width	t _{CL}		35			ns
SCLK Low Width	t _{CL}		35			ns
DIN Setup Time	t _{DS}		45			ns
DIN Hold Time	t _{DH}		0			ns
DOUT Valid Propagation Delay	t _{DOV}	C _L = 50pF		80		ns
CS High Pulse Width	t _{CSW}		20			ns
CLR Pulse Width	t _{CLR}		25			ns
CS Rise to SCLK Rise Setup Time	t _{CS1}		50			ns

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

ELECTRICAL CHARACTERISTICS—Dual Supplies (MAX531 Only)

V_{DD} = 5V ± 10%, V_{SS} = -5V ± 10%, AGND = DGND = 0V, REF_{IN} = 2.048V (external), REF_B = BIPOFF = V_{OUT}, CREFOUT = 33pF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	N		12			Bits
Relative Accuracy	INL	MAX531ACIE			±0.5	LSB
		MAX531IAM			±1	LSB
		MAX531BCIE			±1	LSB
Differential Nonlinearity	DNL	Guaranteed monolithic			±2	LSB
Bipolar Offset Error	V _{OS}	BIPOFF = REF _{IN}			±1	LSB
Bipolar Offset Tempco	TCV _{OS}	BIPOFF = REF _{IN}		3		ppm/°C
Gain Error (Unipolar or Bipolar)	GEU	MAX531_CIE MAX531_IM			±1	LSB
Gain-Error Tempco					±2	ppm/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V _{DD} ≤ 5.5V, -5.5V ≤ V _{SS} ≤ -4.5V		1	200	μV/V
REFERENCE INPUT (REF_{IN})						
Voltage Range			V _{SS} +2		V _{DD} -2	V
Input Resistance		Code dependent, minimum at code 555 hex		40		kΩ
Input Capacitance		Code dependent (Note 4)		10	50	pF
AC Feedthrough		REF _{IN} = 1kHz, 2 V _{pp} -p			-80	dB
REFERENCE OUTPUT (REF_{OUT}—MAX531 only)						
Reference Output Voltage		T _A = +25°C	2.024	2.048	2.072	
		V _{DD} = 5.0V (Note 6)	2.017		2.079	V
		MAX531BC	2.013		2.083	
Temperature Coefficient	TCREF _{OUT}	MAX531ACIE/AMIBM		15	50	ppm/°C
		MAX531BCIE		15	50	ppm/°C
Resistance	PREFOUT	(Note 5)		0.5	2	Ω
Power-Supply Rejection Ratio	PSRR	4.5 ≤ V _{DD} ≤ 5.5V			300	μV/V
Noise Voltage	e _n	0.1Hz to 10kHz			400	μV-p-p
Minimum Required External Capacitor	C _{MIN}			3.3		μF
DIGITAL INPUTS (DIN, SCLK, CS)						
Input High	V _{IH}		2.4			V
Input Low	V _{IL}			0.8		V
Input Current	I _{IN}	V _{IN} = 0V or V _{DD}			±1	μA
Input Capacitance	C _{IN}			8		pF
DIGITAL OUTPUT (DOUT)						
Output High	V _{OH}	I _{SOURCE} = 2mA		V _{DD} - 1		V
Output Low	V _{OL}	I _{SINK} = 2mA			0.4	V

MAX531/MAX538/MAX539

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

ELECTRICAL CHARACTERISTICS—Dual Supplies (MAX531 Only) (continued)

V_{DD} = 5V ± 10%, V_{SS} = -5V ± 10%, AGND = DGND = 0V, REF_{IN} = 2.048V (external), REF_B = BIPOFF = V_{OUT}, CREFOUT = 33pF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE OUTPUT (V_{OUT})						
Output Voltage Range		MAX531(G = 1)		V _{SS} + 2	V _{DD} - 2	V
		MAX531(G = 2)		V _{SS} + 0.4	V _{DD} - 0.4	V
		V _{OUT} = 2V, R _L = 2kΩ			-1	LSB
Output Load Regulation						LSB
Short-Circuit Current	I _{SC}					mA
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR	To ± 1/2LSB, V _{OUT} = 2V	0.15	0.25		V/μs
Voltage-Output Settling Time		Step 000hex to FFFhex		25		μs
Digital Feedthrough		REF _{IN} = 1kHz, 2V _{pp} -p (G = 1)		69		nV-s
Signal-to-Noise plus Distortion	SINAD	REF _{IN} = 1kHz, 2V _{pp} -p (G = 2)		69		dB
POWER SUPPLY						
Positive Supply Voltage	V _{DD}		4.5		5.5	V
Negative Supply Voltage	V _{SS}		-5.5		0	V
Positive Supply Current	I _{DD}	All inputs = 0V or V _{DD} , no load		260	400	μA
Negative Supply Current	I _{SS}	All inputs = 0V or V _{DD} , no load		-120	-200	μA
SWITCHING CHARACTERISTICS						
CS Setup Time	CS _{ST}		20			ns
SCLK Fall to CS Fall Hold Time	CS _{HF}		15			ns
SCLK Fall to CS Rise Hold Time	CS _{HR}		0			ns
SCLK High Width	t _{CH}		35			ns
SCLK Low Width	t _{CL}		35			ns
DIN Setup Time	t _{DS}		45			ns
DIN Hold Time	t _{DH}		0			ns
DOUT Valid Propagation Delay	t _{DOV}	C _L = 50pF		80		ns
CS High Pulse Width	t _{CSW}		20			ns
CLR Pulse Width	t _{CLR}		25			ns
CS Rise to SCLK Rise Setup Time	CS _{ST}		50			ns

Note 2: In single-supply operation, INL and GE calculated from Code 11 to Code 4095. Tested at V_{DD} = 5V.

Note 3: Unipolar Offset Error is an input referred error. For a gain of 1, the output error is 50μV, while for a gain of 2 the output error is 1mV.

Note 4: Guaranteed by design.

Note 5: Tested at I_{OUT} = 100μA. The reference can typically source up to 5mA (see Typical Operating Characteristics).

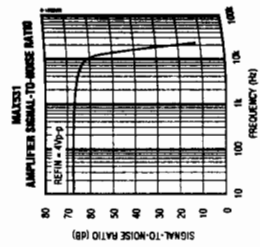
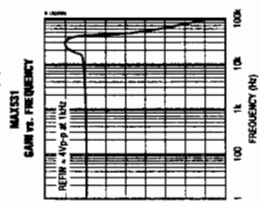
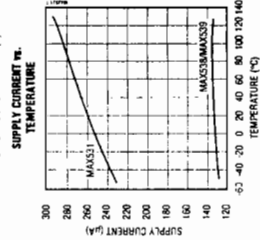
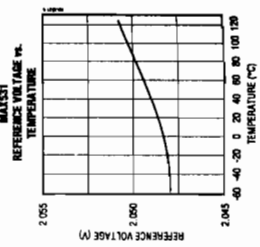
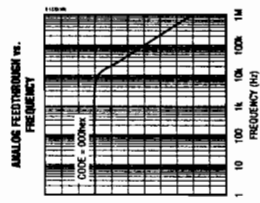
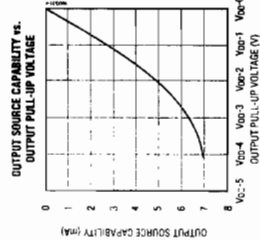
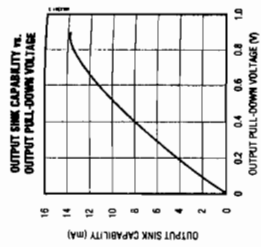
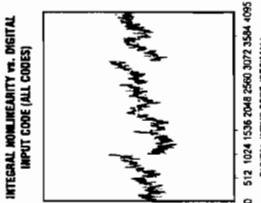
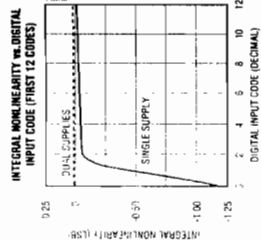
Note 6: MAX531ACIE/AMIBM reference tolerance over temp is guaranteed by 50ppm/°C max temperature coefficient.

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

MAX531/MAX538/MAX539

Typical Operating Characteristics

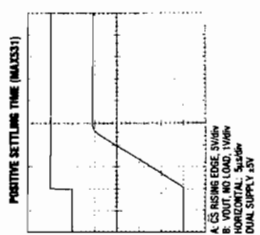
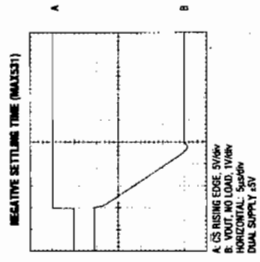
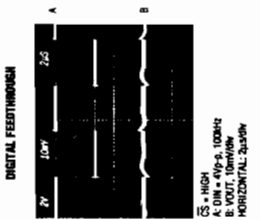
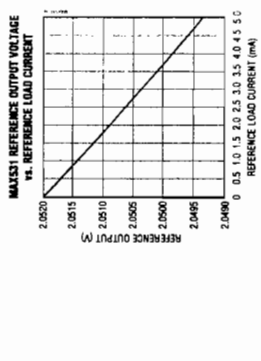
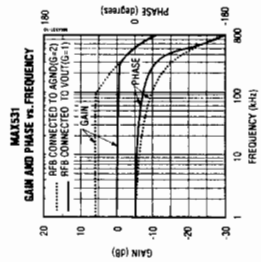
(V_{CC} = +5V, V_{REFIN} = 2.048V, T_A = +25°C, unless otherwise noted)



5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{REFIN} = 2.048V, T_A = +25°C, unless otherwise noted)



5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

Pin Description

PIN	NAME	FUNCTION
MAX531	MAX538/ MAX539	
1	—	Bypass capacitor
2	DIN	Serial data input
3	CLR	Clear. Asynchronously sets DAC register to 000hex.
4	SCLK	Serial clock input
5	CS	Chip select, active low
6	DOUT	Serial data output for daisy-chaining
7	—	Digital ground
8	AGND	Analog ground
9	REFIN	Reference input
10	—	Reference output, 2.048V
11	—	VSS
12	VOOUT	DAC output
13	VDD	Positive power supply
14	—	Feedback resistor

Detailed Description

The MAX531/MAX538/MAX539 use an "inverted" R-2R ladder network with a single-supply CMOS op amp to convert 12-bit digital data to analog voltage levels (see Functional Diagram). The term "inverted" describes the ladder network because the REFIN pin in current-output DACs is the summing junction, or virtual ground, of an op amp. However, such use would result in the output voltage being the inverse of the reference voltage. The MAX531/MAX538/MAX539's topology makes the output the same polarity as the reference input.

An internal reset circuit forces the DAC register to reset to 000hex on power-up. Additionally, a clear (CLR) pin when held low, sets the DAC register to 000hex. CLR operates asynchronously and independently from the chip select (CS) pin.

Buffer Amplifier

The output buffer is a unity-gain stable, rail-to-rail output BICMOS op amp. Input offset voltage and CMRR are trimmed to achieve better than 12-bit performance. Settling time is 25µs to 0.01% of full scale. The output is short-circuit protected and can drive a 2kΩ load with more than 100pF load capacitance.

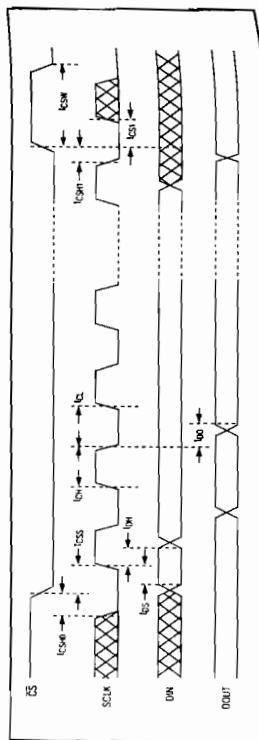


Figure 1. Timing Diagram

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

MAX531/MAX538/MAX539

at code 000hex. REFIN's input capacitance is also code dependent and has a 50pF maximum value at 5V. The codes. Because of the code-dependent nature of the input impedances, a high-quality, low-power, precision amplifier (such as the MAX480 low-power, precision op amp) should be used.

If an upgrade to the internal reference is required, the 2.5V MAX531/538 is suitable. ±15mV initial accuracy, TCVO_{LSB} = 70ppm/°C (max).

Logic Interface

The MAX531/MAX538/MAX539 logic inputs are designed to be compatible with TTL or CMOS logic levels. However, to achieve the lowest power dissipation, the digital inputs with rail-to-rail CMOS logic. With TTL logic levels, the power requirement increases by a factor of approximately 2.

Serial Clock and Update Rate

Figure 1 shows the MAX531/MAX538/MAX539 (min). The maximum serial clock rate is given by 1/(t_{CSH}+t_{CSL}). The maximum 14MHz. The digital update rate is limited by the chip-select period, which is 16 × SCLK periods plus 2 × t_{CS} high pulse width t_{CSW}. This equals a 1.14µs, or 875kHz, update rate. However, the DAC settling time to 12 bits is 25µs, which may limit the update rate to 40kHz for full-scale step transitions.

Applications Information

Refer to Figures 3a and 3b for typical operating connections.

Serial Interface

The MAX531/MAX538/MAX539 use a three-wire serial interface that is compatible with SPI™, CSPI™, and Microwire™ standards as shown in Figures 4 and 5. The DAC is programmed by writing two 8-bit words (see Figure 1 and the Functional Diagram). The MSB of serial data are clocked into the DAC MSB first with bits are not normally needed. They are required only when DACs are daisy-chained. Data is clocked on CS's falling edge while CS is low. The serial input data is held in a 16-bit serial shift register. On CS's rising edge, the 16-bit significant bits are transferred to the DAC register and update the DAC. With CS high, data cannot be clocked into the MAX531/MAX538/MAX539.

The MAX531/MAX538/MAX539 inputs data in 16-bit blocks. The SPI and Microwire interfaces output data in 8-bit blocks, thereby requiring two write cycles to input data to the DAC. The CSPI interface allows variable data input from 8 to 16 bits, and can be loaded into the DAC in one write cycle.

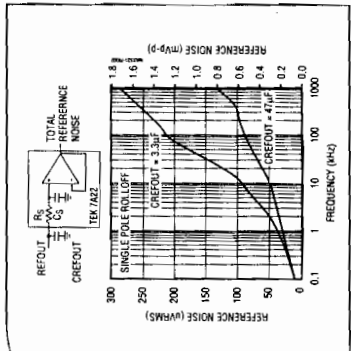


Figure 2. Reference Noise vs. Frequency

Internal Reference (MAX531 only)

To achieve the lowest-power design possible, the DAC ladder resistance has been set to approximately 50kΩ, which allows the internal reference circuit to be biased at about 100µA. This reference voltage is trimmed to 2.048V. In the MAX531, this reference is brought to an external pin and may be gained up or down, inverted, or connected to VDD for a multiplying application. The reference output can be set up to 5mA of external load current, and has an output resistance typically less than 10mΩ (20ms max).

For applications requiring very low-noise performance, connect a 33µF capacitor from REFOUT to AGND. If noise is not a concern, a lower value (3.3µF min) capacitor may be used. To reduce noise further, insert a buffered RC filter between REFOUT and REFIN (Figure 2). The reference bypass capacitor CREFOUT is still required for reference stability. In applications not requiring the reference, connect REFOUT to VDD or use the MAX538 or MAX539 (no internal reference).

External Reference

An external reference in the range (VSS + 2V) to (VDD - 2V) may be used with the MAX531 in single-supply operation. With the MAX538/MAX539 or the MAX531 in single-supply mode, the reference must be positive and may not exceed VDD - 2V. The reference voltage determines the DAC's full-scale output. The DAC input resistance is code dependent and is minimum (40kΩ) at code 555hex and virtually infinite

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

MAX531/MAX538/MAX539

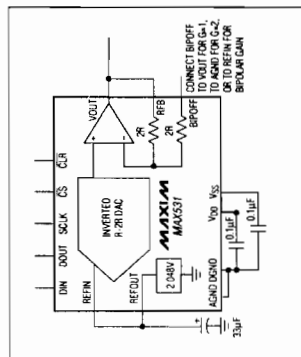


Figure 3a. MAX531 Typical Operating Circuit

Daisy-Chaining Devices
The serial output, DOUT, allows cascading of two or more DACs. The data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width. For low power, DOUT is a CMOS output that does not require an external pull-up resistor. CS is high to input into a high-impedance state when CS is low. When CS is high, DOUT remains in the state of the last data bit.

Any number of MAX531/MAX538/MAX539 DACs can be daisy-chained by connecting the DOUT of one device to the DIN of the next device in the chain. For proper timing, ensure that CS50 (CS low to SCLK high) is greater than $t_{DLY} + t_{DIN}$.

Unipolar Configuration
The MAX531 is configured for a Gain = 1, 0V to +2.048V unipolar output range by connecting BIPOFF and RFB to VOUT (Figure 6). The converter operates from either single or dual supplies in this configuration. See Table 1 for the DAC-latch contents (INPUT) vs. the analog VOUT (output). In this range, 1LSB = REFIN (2⁻¹²). The MAX538 is internally configured for unipolar Gain = 1 operation.

A Gain = 2, 0V to 4.096V unipolar output range is set up by connecting BIPOFF to AGND and RFB to VOUT (Figure 7). Table 2 shows the DAC-latch contents vs. VOUT. The MAX531 operates from either single or dual

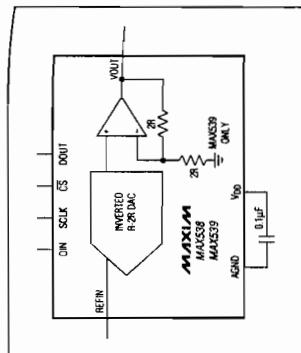


Figure 3b. MAX538/MAX539 Typical Operating Circuit

supplies in this mode. In this range, 1LSB = (2/REFIN)(2⁻¹²) = (REFIN/2⁻¹¹). The MAX539 is internally configured for unipolar Gain = 2 operation.

Bipolar Configuration
A bipolar range is set up by connecting BIPOFF to REFIN and RFB to VOUT, and operating from dual (±5V) supplies (Figure 8). Table 3 shows the DAC-latch contents (INPUT) vs. VOUT (output). In this range, 1LSB = REFIN(2⁻¹¹).

Four-Quadrant Multiplication
The MAX531 can be used as a four-quadrant multiplier by connecting BIPOFF to REFIN, using an offset binary or two's-complement digital code, and using dual power supplies and a bipolar analog input at REFIN within the range $V_{SS} + 2V$ to $V_{DD} - 2V$, as shown in Figure 9.

In general, a 12-bit DAC's output is (D) (VREFIN) (G), where 'G' is the gain (1 or 2) and 'D' is the digital representation of the digital input divided by 2^{12} or 4.096. This formula is precise for unipolar operation. However, for bipolar, two's-complement operation, the MSB is really a polarity bit. No resolution is lost, as there are the same number of steps. The output is shifted from the same number of steps. The range of, for example, 0V to 4.096V (G = 2) to a range of -2.048V to +2.048V.

Keep in mind that when using the DAC as a four-quadrant multiplier, the scale is skewed. Negative -1LSB is -VREFIN, while positive full scale is +VREFIN - 1LSB.

™ SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

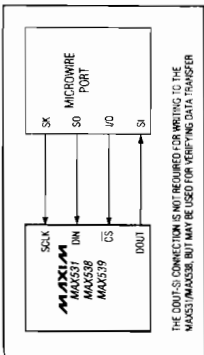


Figure 4. Microwire Connection

THE DOUT-SI CONNECTION IS NOT REQUIRED FOR WRITING TO THE MAX531/MAX538, BUT MAY BE USED FOR VERIFYING DATA TRANSFER.

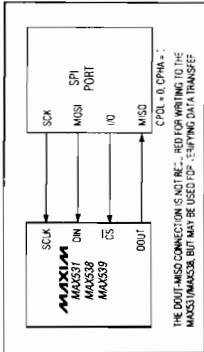


Figure 5. SPI/QSPI Connection

THE DOUT-MISO CONNECTION IS NOT REQUIRED FOR WRITING TO THE MAX531/MAX538, BUT MAY BE USED FOR VERIFYING DATA TRANSFER.

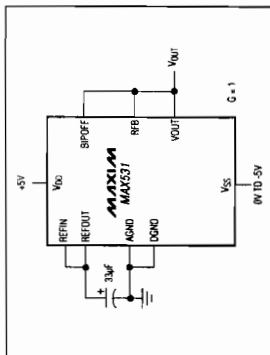


Figure 6. Unipolar Configuration (0V to +2.048V Output)

Table 1. Unipolar Code Table (0V to VREF Output)
Gain = 1

INPUT	OUTPUT
1111 1111 1111	4095 (VREF) 4096
1000 0000 0001	2049 (VREF) 4096
1000 0000 0000	2048 (VREF) 4096 = +VREF/2
0111 1111 1111	2047 (VREF) 4096
0000 0000 0001	1 (VREF) 4096
0000 0000 0000	0V

Table 2. Unipolar Code Table (0V to 2VREF Output)
Gain = 2

INPUT	OUTPUT
1111 1111 1111	4095 +2 (VREF) 4096
1000 0000 0001	2049 +2 (VREF) 4096
1000 0000 0000	2048 +2 (VREF) 4096 = +VREF
0111 1111 1111	2047 +2 (VREF) 4096
0000 0000 0001	1 +2 (VREF) 4096
0000 0000 0000	0V

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

MAX531/MAX538/MAX539

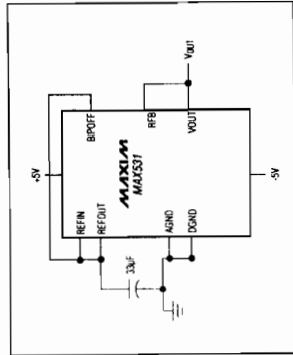


Figure 8. Bipolar Configuration (-2.048V to +2.048V Output)

Table 3. Bipolar Code Table (VREF to -VREF Output)

INPUT	OUTPUT
1111 1111 1111	2047 (+VREF) 2048
1000 0000 0001	1 (+VREF) 2048
1000 0000 0000	0V
0111 1111 1111	1 (-VREF) 2048
0000 0000 0001	2047 (-VREF) 2048
0000 0000 0000	2048 (-VREF) 2048

Single-Supply Linearity

As with any amplifier, the MAX531/MAX538/MAX539's output buffer can be positive or negative. When the offset is positive, it is easily accounted for (Figure 10). However, when the offset is negative, the buffer output cannot follow linearity when there is no negative supply. In that case, the amplifier output (VOUT) remains at ground until the DAC voltage is sufficient to overcome the offset and the output becomes positive. Normally, linearity is measured after accounting for zero error and gain error. Since, in single-supply operation, the actual value of a negative offset is unknown, it cannot be accounted for during test. Additionally, the output buffer amplifier exhibits a nonlinear near-zero output when operating with a single supply. To account for this nonlinearity in the MAX531/MAX538/MAX539, linearity and gain error are measured from code 11 to code 4095. The output buffer's offset and nonlinear behavior do not affect monotonicity, and these DACs are guaranteed monotonic starting with code zero. In dual-supply operation, linearity and gain error are measured from code 0 to 4095.

Power-Supply Bypassing and Ground Management

Best system performance is obtained with printed circuit boards that use separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be connected together at the low-impedance power-supply source.

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

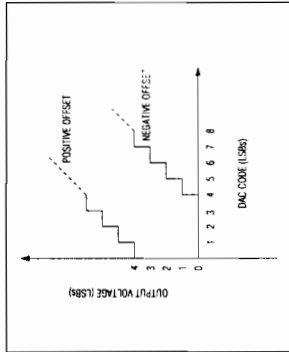


Figure 10. Single-Supply Offset

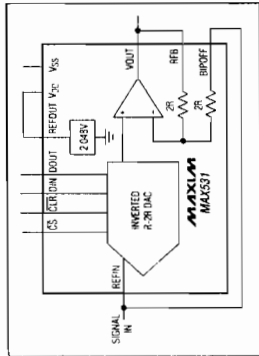


Figure 9. MAX531 Connected as Four-Quadrant Multiplier. The unused REFCUT is connected to VDD.

AC Considerations

Digital Feedthrough

High-speed serial data at any of the digital input or output pins may couple through the DAC package and cause internal stray capacitance to appear at the DAC output as noise, even though CS is held high (see Typical Operating Characteristics). This digital feedthrough is tested by holding CS high transmitting 555hex from DIN to DOOUT.

Analog Feedthrough

Because of internal stray capacitance, higher frequency analog input may couple to the output as shown in the Analog Feedthrough vs. Frequency graph in the Typical Operating Characteristics. It is tested by sweeping an analog input with CS not asserted and DIN set to DOOUT.

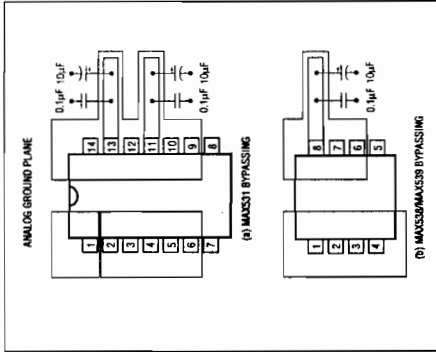


Figure 11. Power-Supply Bypassing

